

PATENT AMENDMENTS SHEET

Maximally Digitized Fractional-N Frequency Synthesizer and Modulator with Maximal Fractional Spurs Removing
Xiaopin Zhang, Strehleranger 3, 81735 Munich, Germany, Tel:+49 89 35465225

TITLE OF INVENTION

Maximally Digitized Fractional-N Frequency Synthesizer and Modulator with
Maximal Fractional Spurs Removing

APPLICATION NUMBER

10/656,762



AMENDMENTS TO THE SPECIFICATION

The paragraph [0029] on page 10 of the specification is amended as follows.

[0029] The algorithm shown in Figure 5 uses the first case detection event to generate the feedback control signal. The ideal feedback error signal is the change of the angle between the two clock hands during one reference period, which is the instantaneous frequency difference between the two signals. If the two comparing bits are the same, as stated above that the angle difference may probably be small, the error signal is sent as zero. Once the first case detection event is triggered by the two different comparing bits, the angle of the state line where the accumulator hand stays will be outputted as the error signal. ~~This error detection algorithm obviously is not absolute accurate since the error signal may always not equal to actual angle difference, no matter the error signal is zero or not zero. However, if the extra angle difference that is not included in one detection could be possibly detected in the following detections with a delay that is much less than the reciprocal of the loop bandwidth, the performance penalty caused by the delay will be acceptable. Keeping the undetected angle difference for the following detection is done by restarting the accumulator hand from the reference line again after a nonzero error signal is generated. In fact, this is equivalent to rotate the accumulator hand by an angle that is equal to the error signal towards the DSFD hand. The angle difference between the two hands after this will be the extra angle difference that is not been detected. In the following operations if the angle difference has evolved large enough to trig another first case detection event, the contribution of that extra~~

PATENT AMENDMENTS SHEET

Maximally Digitized Fractional-N Frequency Synthesizer and Modulator with Maximal Fractional Spurs Removing
Xiaopin Zhang, Strehleranger 3, 81735 Munich, Germany, Tel:+49 89 35465225

angle difference will be eventually included If the error detection is precise, after the error signal is generated the accumulator hand need to be restarted at the position of DSFD hand so that the detection in the following reference cycle will only detect the change of the angle between the two clock hands during those cycles and not include the above detected error signal. In fact, this is equivalent to rotate the accumulator hand with an angle shift that is equal to the error signal towards the DSFD hand. But since the detected error signal is not exactly equal to the angle between the two clock hands, the accumulator hands cannot be restart at the same position where the DSFD hand is. It is only possible to rotate the accumulator hand with the angle of generated error signal, so that for the detection in the following cycle there will be an initial angle difference that equals the phase error not been detected between the two clock hands. Fortunately, this is also the best way to restarting the accumulator hand. This is because that in the following operations if the angle difference has evolved large enough to trig another first case detection event, the contribution of that extra angle difference not been detected in the previous reference cycle will be eventually included. From the view of graphic notation, the accumulator hand will follow the DSFD hand closely as the result of the rotation after each error signal generation. As long as the two clock hands follow each other closely, the undetected phase error will always be very small and all the phase error evolved will be finally detected. Therefore, there will be only some delay to a small part of the phase error in the detection. If the delay is much less than the reciprocal of the loop bandwidth, the performance penalty cause by the delay will be acceptable.